

CLAIMS

1 1. A method for reading data from a memory to achieve reduced jitter, comprising
2 the steps of:
3 applying successive read clock pulses to the memory at a frequency of $x f_n$ where x is a
4 whole integer and f_n is the frequency at which the memory is clocked to write data;
5 applying successive Read Addresses to the memory at a frequency on the order of f_n to
6 identify successive locations in the memory for reading when the memory is clocked with read
7 clocked pulses to enable reading of samples stored at such successive locations; and
8 altering the duration of at least one successive Read Addresses in response to memory
9 usage status to maintain memory capacity within at least one a prescribed threshold.

1 2. The method according to claim 1 further comprising the step of lengthening the
2 duration of the at least one Read Address to repeat reading of a fractional sample.

1 3. The method according to claim 2 further comprising the step of lengthening the
2 duration of more than one Read Address to repeat the reading of more than one fractional
3 sample.

1 4. The method according to claim 1 further comprising the step of shortening the
2 duration of the at least one Read Address to skip reading of a fractional sample.

1 5. The method according to claim 4 further comprising the step of shortening the
2 duration of more than one Read Address to skip reading of more than one fractional sample.

1 6. The method according to claim 1 further comprising the step of applying the
2 successive read clock pulses to the memory at a frequency four times the frequency f_n .

1 7. A system for reading stored data to achieve reduced jitter, comprising:
2 a memory into which data is written and from which data is read;
3 a clock applying successive read clock pulses to the memory at a frequency of $x f_n$ where
4 x is a whole integer and f_n is the frequency at which the memory is clocked to write data;

5 a memory address generator for applying successive Read Addresses to the memory at a
6 frequency on the order of f_n to identify successive locations in the memory for reading when the
7 memory is clocked with read clocked pulses to enable reading of samples stored at such
8 successive locations; and for altering the duration of at least one successive Read Addresses in
9 response to memory usage status to maintain memory capacity within at least one a prescribed
10 threshold.

1 8. The apparatus according to claim 7 wherein the memory address generator
2 lengthens the duration of the at least one Read Address to repeat reading of a fractional sample.

1 9. The apparatus according to claim 8 wherein the memory address generator
2 lengthens the duration of more than one Read Address to repeat the reading of more than one
3 fractional sample.

1 10. The apparatus according to claim 7 wherein the memory address generator
2 shortens the duration of the at least one Read Address to skip reading of a fractional sample.

1 11. The apparatus according to claim 10 wherein the memory address generator
2 shortens the duration of more than one Read Address to skip reading of more than one fractional
3 sample.

1 12. The apparatus according to claim 1 wherein the system clock applies successive
2 read clock pulses to the memory at a frequency four times the frequency f_n .